Gate Insulator Engineering in Top-Gated ITO-Stabilized ZnO TFTs

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Abstract

This work proposes a high-quality type of PECVD SiO_2 stack for TFTs, which contains a layer of SiH_4-sourced PECVD SiO_2 (SiH_4-SiO_2) with a layer of TEOS-sourced PECVD SiO_2 (TEOS-SiO_2) underneath. The issues of high hydrogen content in the SiH_4-SiO_2 and rich hydroxyl groups in the TEOS-SiO_2 were found to be well addressed when the TEOS-SiO_2 was capped by the SiH_4-SiO_2. Fabricated Al/SiO_2/n++ Si capacitors with separate and stacked PECVD SiO_2 dielectrics revealed that the electrical properties of the SiO_2 stacks are superior to their mono-layer counterparts. This is owing to the mutual interactions between hydrogen atoms in the SiH_4-SiO_2 and hydroxyl groups in the TEOS-SiO_2. Top-gated ITO-stabilized ZnO TFTs with stacked gate insulators (GIs) were demonstrated and shown to be free of hysteresis with a fairly high on-off ratio of over 4×10^{10} and extremely sharp subthreshold swing of 87.7 mV/decade. The combination of TEOS-SiO_2 and SiH_4-SiO_2 initiates a strategy to realize reliable GIs for MO TFTs.

1. Introduction

Metal oxide (MO) thin-film transistors (TFTs) have recently exhibited their potential in fields like active-matrix flat-panel displays (AM-FPDs) [1]-[3], advanced sensors [4]-[6] and integrated circuits (ICs) [7]-[9]. For TFTs, especially those with process-sensitive MO active channels (ACs), the gate insulator (GI) is one of the core device components. The proper adoption of GI materials [10],[11] and deposition processes [12],[13] will directly affect the quality of GIs and GI/AC interfaces, which are further relevant to device performance and reliability [11],[14],[15]. Owing to its merits including a mature technique, low cost, and high quality and throughput, SiO_2 created using the plasma-enhanced chemical vapor deposition (PECVD) technique is generally chosen as the GI layer or one layer of a GI stack. Among PECVD SiO_2, there are two popular embodiments. One is based on a gaseous silane (SiH_4) source (SiH_4-SiO_2), and the other uses a liquid tetraethyl-orthosilicate (TEOS) precursor (TEOS-SiO_2). However, there always exist some undesirable issues when they are separately employed as the GIs of MO TFTs. It is known that the content of hydrogen (H) in SiH_4-SiO_2 is quite high, which can easily diffuse into the ACs [16]-[18]. These hydrogen atoms can donate electrons by forming M-OH bonds with metal cations [19], or generate subgap states near the valence band maximum (VBM) by forming M-H bonds and hence degrade negative bias illumination stress stability [20]. On the other hand, hydroxyl (OH) groups and water are very rich in TEOS-SiO_2 [18]. It is reported that OH groups are able to induce electric dipoles at the GI/AC interfaces of MO TFTs, resulting in remarkable hysteresis [21]. Meanwhile, water molecules can serve as either electron donors or acceptor-like trap sites with regard to the thickness of MO thin films [22].

In order to address the abovementioned drawbacks, we have demonstrated a type of PECVD SiO_2 stack that includes a SiH_4-SiO_2 layer with a TEOS-SiO_2 layer underneath. The content of H and OH groups in the separate and stacked SiO_2 thin films were first measured and compared. Next, related Al/SiO_2/n++ Si capacitors were fabricated, then investigated in terms of leakage current density and capacitance density. The electrical properties of the dual-layer SiO_2 were found to be enhanced compared with its mono-layer counterparts. Finally, top-gated MO TFTs incorporating the stacked GIs were successfully fabricated, and exhibited good electrical performance.

2. Fabrication Processes

The schematic of the top-gated MO TFTs in this work is shown in Fig. 1(a). The device substrates are 4-inch p-type Si wafers coated with 500-nm-thick thermally grown SiO_2. Initially, 50-nm-thick ITO source/drain (S/D) electrodes were sputtered and patterned. Then, ITO-stabilized ZnO thin films were deposited at room temperature, with a thickness of 50 nm. The detailed sputtering conditions are described elsewhere [23]. Next, a 1/2000 molar aqueous hydrofluoric acid solution was used as the AC wet etchant after photolithography. Afterwards, 150-nm-thick TEOS-SiO_2 or SiH_4-SiO_2 GIs, and GI stacks of 50-nm-thick SiH_4-SiO_2 with 100-nm-thick TEOS-SiO_2 underneath were deposited using the PECVD technique at 300°C. Note that it is the TEOS-SiO_2 layer that forms the interfaces with the ACs in the TFTs with the stacked GIs. For the TEOS-SiO_2 deposition, the TEOS cylinder was kept at 40°C, and the source was carried into the chamber using Ar gas. The gas flow rate of the N_2O/O_2/Ar, pressure and RF power were 200/200/30 sccm, 220 mTorr and 30 W, respectively. For the SiH_4-SiO_2 deposition, the gas flow rate of the $SiH_4/N_2/N_2O$, pressure and RF power were 8/400/1425 sccm, 900 mTorr and 60 W, respectively. Then, the gate electrodes (GEs) were made of sputtered and dry-etched Al with a thickness of 300 nm. Finally, the SiO_2 regions above the S/D electrodes were removed for testing using

reactive ion etching (RIE) in CHF_3 plasma, followed by post-annealing at 300 °C in air.

The schematic of the fabricated Al/SiO_2/n++ Si capacitors is shown in Fig. 1(b). To fabricate the capacitors, 4-inch heavily doped n-type (n++) Si wafers were employed as substrates and rear electrodes. Then, 150-nm-thick TEOS-SiO_2 or SiH_4-SiO_2 mono-layer dielectrics, or 100-nm-thick TEOS-SiO_2 plus 50-nm-thick SiH_4-SiO_2 stacked dielectrics were deposited on n++ Si wafers. The front electrodes are made of 300-nm-thick sputtered and patterned Al. Last, the Al/SiO_2/n++ Si capacitors were post-annealed at 300 °C in air. The electrical characteristics of the TFTs and the capacitors were measured in a dark probe station using a semiconductor parameter analyzer (B1500, Keysight) and an LCR meter (E4980, Agilent). For Fourier transform infrared spectroscopy (FTIR, Vertex 70 Hyperion 1000, Bruker) and secondary ion mass spectrometer (SIMS, PHI 7200, Physical Electronics) characterizations, the structures and preparation of samples were similar to those of the capacitors but without front electrodes.

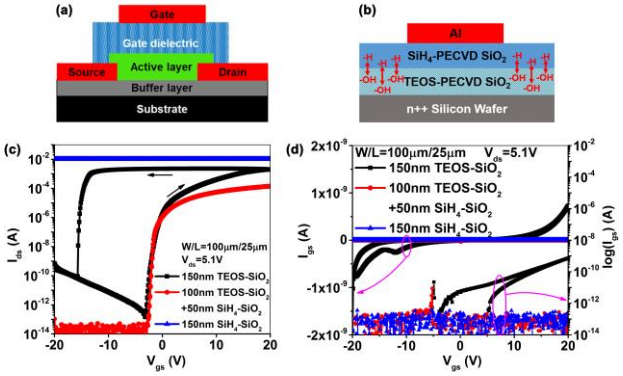

Fig. 1. The schematic of (a) the top-gated MO TFTs with different GIs and (b) the Al/SiO_2/n++ Si capacitors with different dielectrics. The typical (c) I_{ds}-V_{gs} and (d) I_{gs}-V_{gs} curves of the top-gated MO TFTs with different GIs.

3. Results and Discussion

Fig. 1(c) plots the typical transfer curves of the top-gated MO TFTs with different GIs. The devices with only SiH_4-SiO_2 GIs are short-circuited, even though the post-annealing time was extended to >10 h (not shown here). The SIMS spectra in Fig. 2(a) reveal the level of H content in different SiO_2 thin films. The spectra have been calibrated using the relatively stable SiO_2^-signal as a reference. It is obvious that the H content in the SiH_4-SiO_2 is much higher than that in the mono-layer TEOS-SiO_2 and the TEOS-SiO_2 plus SiH_4-SiO_2 stacks. Thus, more hydrogen atoms may diffuse into the ACs and donate a larger number of electrons [16]-[19]. Moreover, there is also a Si-doping phenomenon in our hybrid-phase microstructural ITO-stabilized ZnO thin films during SiH_4-SiO_2 deposition, which enables the ACs to be durably conductive [23]. On the other hand, for the TFTs with only TEOS-SiO_2 GIs, a clear anti-clockwise hysteresis is observed after a cyclic sweep, and the threshold voltage shift (ΔV_{th}) reaches as high as -14.3 V. It is suggested that the large amount of electric dipoles induced by the OH groups at the GI/AC interfaces are responsible for this phenomenon [21]. The FTIR spectra in Fig. 2(b) verify our inference. The IR absorption of the mono-layer TEOS-SiO_2 within the OH-related band (2500~3645 cm^{-1}) is significantly stronger than that of the other SiO_2 thin films. Additionally, the off-state current (I_{off}) in the TFTs based on the individual TEOS-SiO_2 GIs is comparable to their gate leakage (I_{gs}) in Fig. 1(d), so their electrical quality should be the worst among the three types of SiO_2 GIs in this work.

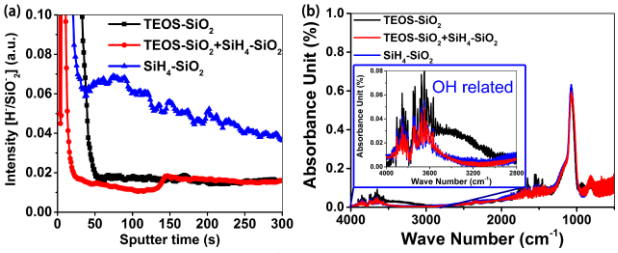

Fig. 2. (a) The SIMS spectra of H- species in TEOS-SiO_2, SiH_4-SiO_2, and TEOS-SiO_2 plus SiH_4-SiO_2 stacks. The signal intensity of the H-species is calibrated using the relatively stable SiO_2- signal as a reference. (b) The FTIR spectra of TEOS-SiO_2, SiH_4-SiO_2, and TEOS-SiO_2 plus SiH_4-SiO_2 stacks. Inset: the specific IR absorption information within the OH-related band.

Unlike the TFTs employing the separate GIs, those with the stacked GIs have substantially different behaviors. Though a layer of SiH_4-SiO_2 is involved, these TFTs can be operated normally, and their turn-on voltage exhibits little shift when compared with the devices with only TEOS-SiO_2 GIs (Fig. 1(c)). Thus, the impacts of the H and Si dopants, which may be blocked by the underlying 100-nm-thick TEOS-SiO_2, on the ACs along with the SiH_4-SiO_2 deposition are slight. However, the existence of the TEOS-SiO_2 does not bring any hysteresis issues at all. This is because the OH group content in the TEOS-SiO_2 plus SiH_4-SiO_2 stacks approaches that in mono-layer SiH_4-SiO_2, which is far lower than that in individual TEOS-SiO_2 layers according to Fig. 2 (b). But the decrease of OH groups is hard to simply explain by a thinner TEOS-SiO_2 layer in the stacks, and there must be other reasons. In Fig. 2(a), the H^- signal before 150 s represents the H content in the upper SiH_4-SiO_2 layer of the stacks. Apart from surface contaminations, its intensity is obviously weaker than that in the mono-layer SiH_4-SiO_2. Therefore, both H and OH traps in the stacks are actually reduced compared with their individual counterparts. This is favorable to realize PECVD SiO_2 GIs with less traps and higher quality. One plausible explanation for the improvement is that excess hydrogen atoms in the SiH_4-SiO_2 and hydroxyl groups in the TEOS-SiO_2 can diffuse mutually. They will interact and even annihilate each other, then form water molecules that can be removed during the PECVD and the following post-annealing processes, as illustrated in Fig. 1(b).

Furthermore, the separate and stacked SiO_2 are investigated as capacitor dielectrics. Fig. 3(a) shows leakage current density as a function of the electric field intensity that is applied on the Al/SiO_2/n++ Si capacitors. Although TEOS-SiO_2 occupies the majority of the dielectric stacks, the leakage current of the corresponding capacitors is remarkably decreased when compared with the capacitors with only TEOS-SiO_2 dielectrics. Meanwhile, the leakage current level is comparable to that

of the individual SiH_4-SiO_2 based capacitors. In addition, it is also found that the capacitors with the dielectric stacks are equipped with the highest critical electric field intensity for soft breakdown, indicating they have the fewest traps studied among the three kinds of capacitors in this work. Furthermore, the capacitance densities of the capacitors with 150-nm-thick dielectrics are measured at 100 kHz. As shown in Fig. 3(b), when the dielectric material is the TEOS-SiO_2, SiH_4-SiO_2, and TEOS-SiO_2 plus SiH_4-SiO_2 stacks, the average capacitance densities are 30.09±0.05, 25.55±0.01, and 28.64±0.02, respectively. Since the TEOS-SiO_2 is thicker than the SiH_4-SiO_2 in the stacks, the result of the stacked capacitors is closer to that of the individual TEOS-SiO_2 based capacitors.

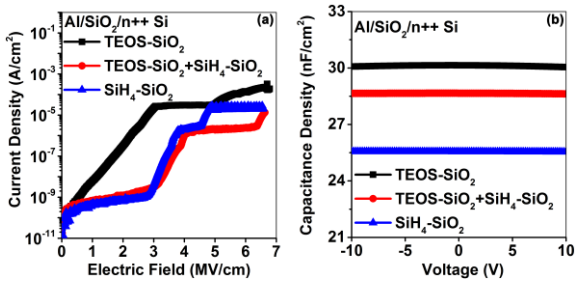

Fig. 3. (a) Leakage current density as a function of electric field intensity that is applied on the Al/SiO_2/n++ Si capacitors. (b) C-V characteristics of the Al/SiO_2/n++ Si capacitors. The 500-nm-thick SiO_2 dielectric herein is TEOS-SiO_2, SiH_4-SiO_2, or TEOS-SiO_2 plus SiH_4-SiO_2 stacks.

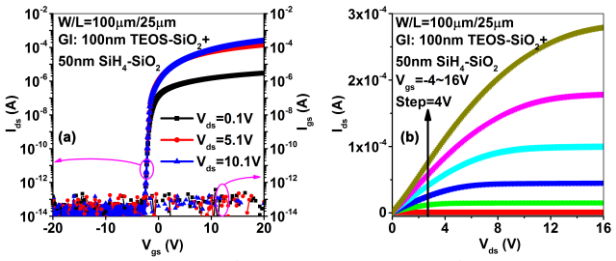

Fig. 4. The typical (a) transfer and (b) output curves of the top-gated MO TFTs with the stacked GIs containing 100-nm-thick TEOS-SiO_2 and 50-nm-thick SiH_4-SiO_2. The width and length of ACs are 100 μm and 25 μm, respectively.

Fig.4 plots the typical transfer and output curves of the top-gated MO TFTs with the stacked GIs containing 100-nm-thick TEOS-SiO_2 and 50-nm-thick SiH_4-SiO_2. Due to the low free carrier concentration of the ACs and the low leakage current of the stacked GIs, I_{off} is low enough to approach the measurement limit. Thus, the devices can be operated with a fairly high on-off ratio of over 4×10^{10}. In addition, their subthreshold swing (SS) reaches as low as 87.7 mV/decade. Then, the total trap density (N_t) in the AC bulks and at the stacked GI/AC interfaces can be calculated according to the following equation [10],

$$N_t = \left[\frac{q \cdot SS \cdot \log(e)}{kT} - 1\right]\frac{C_{ox}}{q}, \quad (1)$$

where q, k, T, and C_{ox} are the electron charge, Boltzmann's constant, absolute temperature and gate capacitance density, respectively. The extracted result is 2.63×10^{11} cm^{-2} eV^{-1}. In the TFTs with the individual TEOS-SiO_2 GIs, their SS and N_t are 212 mV/decade and 6.49×10^{11} cm^{-2} eV^{-1}, respectively. Thus, the GI/AC interfaces can be optimized thanks to the stacked GIs.

4. Conclusions

In this work, it is found that both high H content in SiH_4-SiO_2 and rich OH groups in TEOS-SiO_2 can decrease when two PECVD SiO_2 layers are stacked together. This might be attributable to the mutual interactions between H and OH groups during the 300°C PECVD and post-annealing processes. The developed SiO_2 stacks exhibited strengthened electrical properties. Fabricated top-gated MO TFTs with stacked GIs were free of hysteresis with a fairly high on-off ratio and extremely sharp SS. The combination of TEOS-SiO_2 and SiH_4-SiO_2 provides a strategy to realize reliable GIs for MO TFTs.

References

[1] E. Fortunato, P. Barquinha, and R. Martins, *Adv. Mater.*, vol. 24, no. 22, pp. 2945-2986.

[2] C. I. Park, M. Seong, M. A. Kim, D. Kim, H. Jung, M. Cho, S. H. Lee, H. Lee, S. Min, J. Kim, and M. Kim, *J. Soc. Inf. Display*, vol. 26, no. 5, pp. 287-295.

[3] Y. Hara, T. Kikuchi, H. Kitagawa, J. Morinaga, H. Ohgami, H. Imai, T. Daitoh, and T. Matsuo, *J. Soc. Inf. Display*, vol. 26, no. 3, pp.169-177.

[4] S. Jeon, S. E. Ahn, I. Song, C. J. Kim, U. I. Chung, E. Lee, I. Yoo, A. Nathan, S. Lee, K. Ghaffarzadeh, and J. Robertson, *Nat. Mater.*, vol. 11, no. 4, p. 301.

[5] K. Myny and S. Steudel, in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, USA, Jan./Feb. 2016, pp. 298-299.

[6] D. Geng, S. Han, H. Seo, M. Mativenga, and J. Jang, *IEEE Sens. J.*, vol. 17, no. 3, pp. 585-586.

[7] H. Kim, S. Jeon, M. J. Lee, J. Park, S. Kang, H. S. Choi, C. Park, H. S. Hwang, C. Kim, J. Shin, and U.I. Chung, *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3820-3828.

[8] A. Isobe, H. Tamura, K. Kato, T. Ohmaru, W. Uesugi, T. Ishizu, T. Onuki, K. Ohshima, T. Matsuzaki, A. Hirose, and Y. Suzuki, in *Proc. Symp. VLSI Circuits*, Honolulu, USA, Jun. 2014, pp. 1-2.

[9] K. Kaneko, N. Inoue, S. Saito, N. Furutake, H. Sunamura, J. Kawahara, M. Hane, and Y. Hayashi, in *Proc. Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2011, pp. 7.4.1-7.4.4, doi: 10.1109/IEDM.2011.6131507

[10] C. J. Chiu, S. P. Chang, and S. J. Chang, *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1245-1247.

[11] P. Ma, L. Du, Y. Wang, R. Jiang, Q. Xin, Y. Li, and A. Song, *Appl. Phys. Lett.*, vol. 112, no. 2, p. 023501.

[12] J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage Jr, X. H. Zhang, and B. Kippelen, *Appl. Phys. Lett.*, vol. 94, no. 14, p. 142107.

[13] T. Rembert, C. Battaglia, A. Anders, and A. Javey, *Adv. Mater.*, vol. 27, no. 40, pp. 6090-6095.

[14] K.H. Ji, J. I. Kim, Y. G. Mo, J. H. Jeong, S. Yang, C. S. Hwang, S. H. K. Park, M. K. Ryu, S. Y. Lee, and J. K. Jeong, *IEEE Electron Device Lett.*, vol. 31, no. 12, pp.1404-1406.

[15] J. M. Lee, I. T. Cho, J. H. Lee, W. S. Cheong, C. S. Hwang, and H. I. Kwon, *Appl. Phys. Lett.*, vol. 94, no. 22, p. 222112.

[16] S. E. Liu, M. J. Yu, C. Y. Lin, G. T. Ho, C. C. Cheng, C. M. Lai, C. J. Lin, Y. C. King, and Y. H. Yeh, *IEEE Electron Device Lett.*, vol. 32, no. 2, pp.161-163.

[17] K. S. Son, T. S. Kim, J. S. Jung, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, J. Y. Kwon, S. Y. Lee, and J. M. Kim, in *SID Symp. Dig. Tech. Papers*, vol. 39, no. 1, pp. 633-636.

[18] *Handbook of thin film deposition*, K. Seshan and D. Schepis, eds., Amsterdam, Boston, Waltham: William Andrew Press, 2012.

[19] T. Kamiya, and H. Hosono, *ECS Trans.*, vol. 54, no. 1, pp. 103-113.

[20] J. Bang, S. Matsuishi, and H. Hosono, *Appl. Phys. Lett.*, vol. 110, no. 23, p. 232105.

[21] L. Lu, J. Li, and M. Wong, *IEEE Electron Device Lett.*, vol. 35, no. 8, pp. 841-843.

[22] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo, and H. D. Kim, *Appl. Phys. Lett.*, vol. 92, no. 7, p. 072104.

[23] S. Deng, R. Chen, G. Li, Z. Xia, M. Zhang, W. Zhou, M. Wong, and H. S. Kwok, *IEEE Electron Device Lett.*, vol. 38, no. 12, pp.1676-1679.