Self-Aligned Hybrid-Phase Microstructural ITO-Stabilized ZnO TFTs Achieved via a Combination of PECVD Processes

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ABSTRACT

The hybrid-phase microstructural ITO-stabilized ZnO thin films capped by silane-based or TEOS-based PECVD SiO_2 presented significantly different conductivity after O_2 annealing treatment. Via a combination of differentiated PECVD and O_2 annealing processes, the self-aligned coplanar TFTs with thermally stable conductive source/drain regions were fabricated, which exhibited fairly high electrical characteristics and reliability.

INTRODUCTION

Metal oxide (MO) semiconductors are of increasing interest as thin-film transistor channels, considering their advantages such as low manufacturing costs/temperature, excellent optical transparency, and reasonable electrical properties. Particularly in large-area high-resolution display as well as flexible/wearable display scenario, MO TFTs are regarded as one of best candidates for backplanes [1-2]. So far, MO TFTs with general staggered architecture have been intensively investigated and well optimized. However, the overlap between gate and source/drain (S/D) electrodes is inevitable, which results in the parasitic capacitance, and hence the signal RC delay of TFT-based circuit. Besides, for organic light-emitting diode displays, the capacitive coupling also affects the kickback/feedthrough voltage, so that the luminescence uniformity will be deteriorated [3]. In order to avoid the drawbacks of parasitic capacitance, a self-aligned coplanar structure is always adopted. Such structure is creatively designed to save one photolithography step, however, extra processes such as ion doping [4-5] and plasma treatment [3, 6-7] are necessarily introduced during the formation of conductive S/D regions.

The hybrid-phase microstructural ITO-stabilized ZnO is one of high-performance TFT channel candidates proposed by our group recently [8-9]. In this paper, we found an exclusive feature when investigating such material. That is, the hybrid-phase microstructural ITO-stabilized ZnO thin films capped by silane (SiH_4)-based and tetraethyl orthosilicate (TEOS)-based PECVD SiO_2 (aka SiH_4-SiO_2 and TEOS-SiO_2) would present significantly different electrical conductivity after O_2 annealing treatment. Then, by employing a combination of these two PECVD as well as differentiated O_2 annealing processes, the self-aligned coplanar TFTs with the hybrid-phase microstructural ITO-stabilized ZnO channels and the thermally stable S/D regions could be successfully fabricated. The devices exhibited relatively high electrical characteristics and reliability. Meanwhile, since the S/D regions could become conductive during the deposition of SiH_4-SiO_2 inter layer dielectric, any other additional processes to enhance conductivity could be eliminated.

EXPERIMENTAL

The whole processes of self-aligned coplanar TFTs started from 4-inch p-type silicon wafers coated with 500-nm-thick thermally oxidized SiO_2. A 50-nm-thick ITO-stabilized ZnO active layer was then deposited by co-sputtering ITO and ZnO target under a working pressure of 3 mTorr. The dc power for ITO target and rf power for ZnO target were set as 120 W and 150 W, respectively. Next, it was patterned into active islands by wet etch in diluted hydrofluoric acid, followed by 150-nm-thick SiO_2 gate insulator deposition using TEOS-based PECVD. The TEOS source cylinder was kept at 40 °C; the gas flow rate of N_2O/O_2/Ar were 200/200/30 sccm; the temperature, pressure and power for deposition were 300 °C, 220 mTorr and 30 W, respectively. Afterwards, 200-nm-thick Al was sputtered and patterned as gate electrodes, which was followed by photoresist removal. The gate electrodes then acted as hard mask for the definition of self-aligned coplanar architecture, and the S/D regions were exposed by dry etching TEOS-SiO_2 above. After O_2 annealing at 300 °C for 2h, 150-nm-thick inter layer dielectric was deposited using SiH_4-based PECVD. The carrier gases included 8 sccm SiH_4/400 sccm N_2/1425 sccm N_2O; the temperature, pressure and working power were 300 °C, 900 mTorr and 60 W, respectively. At this moment, the S/D regions became conductive. Next, contact holes were opened using CHF_3 plasma,

followed by test pad deposition and patterning. At last, another O_2 post-annealing treatment was carried out at 300 °C for 2h. The electrical conductivity of various thin films as well as the electrical characteristics of TFTs were measured in the probe station using a semiconductor parameter analyzer (Agilent 4156C). In order to analyze the depth profile of species in thin film stacks, the secondary ion mass spectrometer (SIMS, PHI 7200, Physical Electronics) characterization was employed.

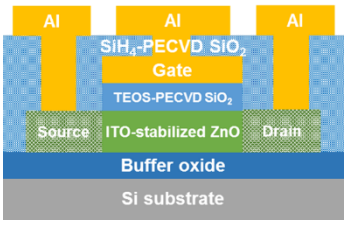

Figure 1. The schematic of self-aligned coplanar TFTs involved in a combination of SiH_4-based and TEOS-based PECVD processes.

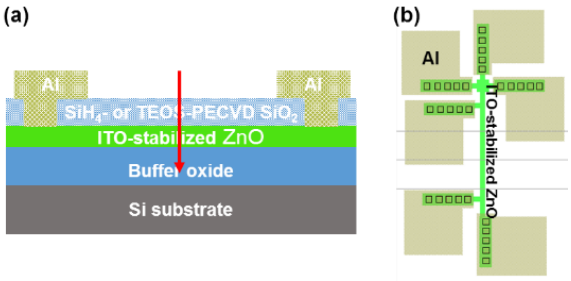

Figure 2. (a) The cross-sectional and (b) plan-view schematic of cross-bridge structure, where the hybrid-phase microstructural ITO-stabilized ZnO thin films are capped by SiH_4-SiO_2 or TEOS-SiO_2 layer.

Table 1. Resistivity of the hybrid-phase microstructural ITO-stabilized ZnO films capped by SiH_4-SiO_2 or TEOS-SiO_2 layer after different O_2 annealing time

Annealing time (h)	0	2	4	6
Resistivity of SiH_4-SiO_2 capped samples (Ω*cm)	1.45e-3	1.39e-2	1.56	8.08
Resistivity of TEOS-SiO_2 capped samples (Ω*cm)	1.09e-2	3.56	1.98e3	2.14e3

RESULTS

Table 1 lists the resistivity of the hybrid-phase microstructural ITO-stabilized ZnO films capped by 150-nm-thick SiH_4-SiO_2 or TEOS-SiO_2 layer after different O_2 annealing time. The results were obtained by measuring the cross-bridge structure, as shown in Figure 2. It can be found that the thin films with either as-deposited SiH_4-SiO_2 or TEOS-SiO_2 are conductive, but the SiH_4-SiO_2 capped samples own less resistivity compared with the TEOS-SiO_2 capped ones. Figure 3(a) presents the depth profile of hydrogen species (along the arrow in Figure 2(a)) in various thin film stacks. A hydrogen accumulation phenomenon is observed at the interface between the PECVD SiO_2 and the hybrid-phase microstructural ITO-stabilized ZnO. Although the relative hydrogen concentration in TEOS-SiO_2 capped samples (mainly in H_2O and Si-OH form) is higher than that in SiH_4-SiO_2 capped samples (mainly in Si-H form), more portion of hydrogen in latter case may act as shallow donors and contribute to the more conductive hybrid-phase microstructural ITO-stabilized ZnO underneath. With time extension of O_2 annealing treatment, both samples become less conductive. However, the resistivity of TEOS-SiO_2 capped samples returns to the initial level after 4h O_2 annealing, whereas it is nearly three orders of magnitude lower for the SiH_4-SiO_2 capped samples. The resistivity increase phenomenon with the rise of O_2 annealing time could be presumably attributed to oxygen deficiency compensation and hydrogen species diffusion out of thin films, as claimed in many self-aligned coplanar MO TFTs with hydrogen doped S/D regions [3, 8-9].However, the resistivity difference between these two PECVD processed thin films needs to be explained. Thus, SIMS characterization with regard to a certain of related species was further conducted. Notably, there is inter-diffusion phenomenon at the interface between the PECVD SiO_2 and the hybrid-phase microstructural ITO-stabilized ZnO, and the degree in SiH_4-SiO_2 capped samples is much more significant. Referring to reference [10], silicon ions are possible to substitute the site of zinc ions and release free carriers in ZnO. That means silicon impurity can behave like aluminum impurity and act as an effective donor in ZnO. Therefore, the silicon-doping effect herein is also believed to gain the conductivity of the SiH_4-SiO_2 capped hybrid-phase microstructural ITO-stabilized ZnO thin films.

According to Table 1, it is noted that the resistivity of TEOS-SiO_2 capped samples with 2h O_2 annealing treatment (1.39×10^{-2} Ω*cm) behaves obviously different compared with that of SiH_4-SiO_2 capped samples with 4h O_2 annealing treatment (1.98×10^{3} Ω*cm). If such two types of PECVD SiO_2 could be employed as gate insulator layers and inter layer dielectric of TFTs, respectively, it is potential to fabricate self-aligned coplanar TFTs with the hybrid-phase microstructural ITO-stabilized ZnO channels. The detailed processes are described in Experimental section above.

As shown in Figure 4, the typical transfer and output curves of self-aligned coplanar TFTs fabricated in this work are plotted. Herein, the devices exhibit fairly high electrical performance with an average linear field-effect mobility of 15.84 cm^2/Vs, threshold voltage of -1.75 V, subthreshold swing of 88 mV/decade, as well as on-off ratio of over 10^7. Unsatisfactorily, such n-channel TFTs are operated in depletion mode, which are not welcomed in low power consumption applications. This is partially related to the hydrogen species

diffusion into channel regions, and more negative threshold voltage is required to deplete the free carriers. Replacing Al gate electrode by ITO is possible to tune the current TFTs towards enhancement-mode devices, and the related work is under progress and will be presented in the future. According to the output curves, the clear pinch-off and the saturation of I_{ds} at high V_{ds} reflect that transistor channels can be effectively controlled by the gate and drain. Frankly speaking, there is a slight crowding effect at low V_{ds}, which indicates the imperfect S/D contacts. However, considering the O_2 post-annealing treatment for several hours, these devices still perform more thermally stable compared with other general MO TFTs owning hydrogen-doped S/D regions [4]. In this aspect, it also verifies that the mechanism for conductive S/D regions herein is not limited by involving hydrogen species, but silicon doping effect.

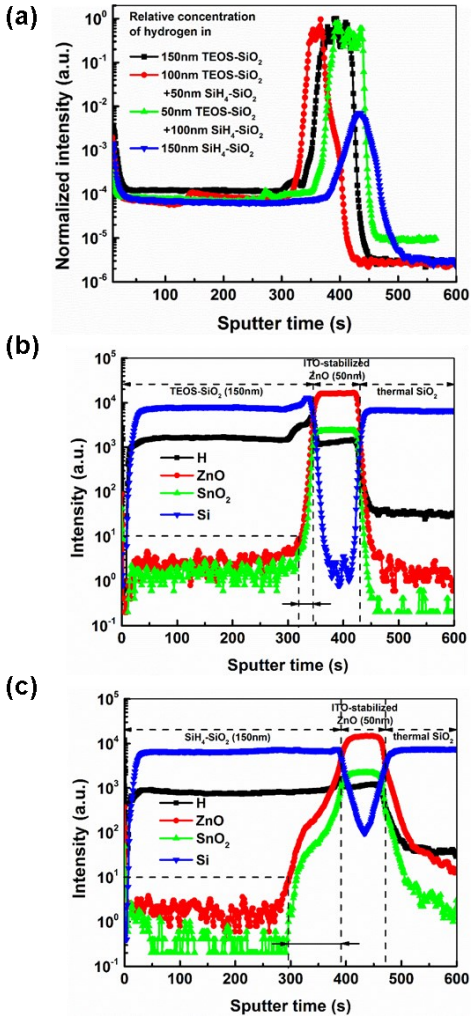

Figure 3. (a) The depth profile of hydrogen species in the hybrid-phase microstructural ITO-stabilized ZnO thin films capped by various combination of SiH_4-SiO_2 and TEOS-SiO_2 layers. The depth profile of some other related species in (b) SiH_4-SiO_2 capped and (c) TEOS-SiO_2 capped samples.

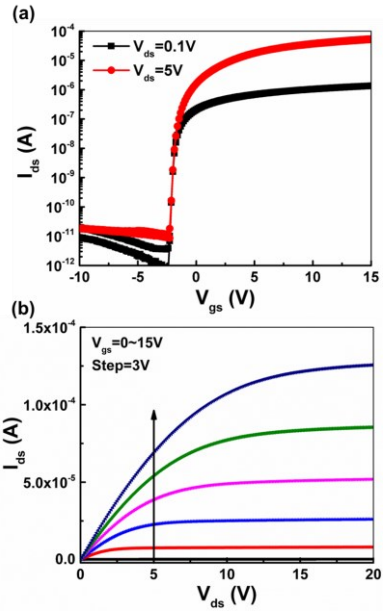

Figure 4. The (a) transfer and (b) curves of self-aligned coplanar TFTs in this work.

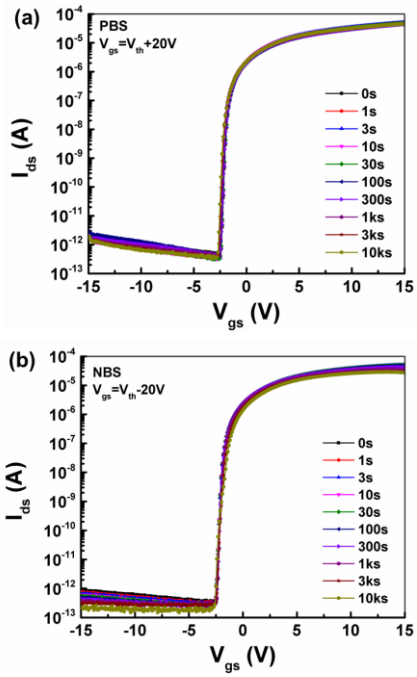

Figure 5. Transfer curve variation of self-aligned coplanar TFTs under (a) NBS and (b) PBS tests for 10 000 s.

Furthermore, the excellent electrical reliability of self-aligned coplanar TFTs under NBS/PBS tests are shown in Figure 5. The V_{ds} is kept at 5 V, and the applied V_{gs} for NBS and PBS are set to (V_{th}-20) V and (V_{th}+20) V for 10 000 s, respectively. There is no stretch-out phenomena observed in the subthreshold region of transfer curves, which means little defects are generated during the stress tests. Meanwhile, all the transfer curves are almost overlapped, except for a slight on-state current decrease under NBS tests due to S/D region degradation.

CONCLUSIONS

The hybrid-phase microstructural ITO-stabilized ZnO thin films capped by TEOS-based or SiH_4-based PECVD SiO_2 layer would perform significantly different conductivity variation trend after O_2 annealing treatment. The TEOS-SiO_2 capped thin films returned initially high resistive state, whereas the SiH_4-SiO_2 capped thin films remained low resistive state eventually due to hydrogen as well as silicon doping effect. Via a combination of differentiated PECVD processes and O_2 annealing steps, the self-aligned coplanar TFTs with the hybrid-phase microstructural ITO-stabilized ZnO channels and the thermally stable conductive S/D regions were successfully fabricated. The devices exhibited fairly high electrical performance and reliability.

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